REMARKS

This Amendment is filed in response to the Office Action dated June 24, 2003, which has a shortened statutory period set to expire September 24, 2003. Applicants have amended Claims 1-20. No new matter is added. Applicants respectfully submit that Claims 1-20, as amended, are patentable over the cited art.

Specifically, Claim 1, as amended, now recites:

    a) placing cells of a circuit design by use of non-direct timing driven processes;
    b) providing routing information associated with said cells;
    c) performing an incremental placement of said cells using said routing information;
    d) placing said cells by use of direct timing driven placement processes; and
    e) repeating b) and c) after d) to optimize placement of said cells.

Applicants respectfully submit that Groenveld fails to disclose or suggest these limitations. Specifically, Groenveld teaches that a single detailed placement (Col. 6, lines 49-51) is performed after a coarse placement step that need not be timing driven (Col. 7, lines 20-22) and an electrical optimization step that includes satisfying predetermined timing constraints (Col. 6, lines 8-10). Because Groenveld fails to teach Applicants' recited method for placing circuit elements on an integrated circuit, Applicants request reconsideration and withdrawal of the rejection of Claim 1.

Claim 2 depends from Claim 1 and therefore is patentable for at least the reasons presented for Claim 1. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claim 2.

Claim 3, as amended, now recites:

a) placing cells of a circuit design by
use of non-direct timing driven processes;
b) routing wiring to connect said cells,
thereby generating a layout;
c) minimizing required signal timing
within said layout;
d) performing an incremental placement of
said cells;
e) placing said cells by use of direct
timing driven placement processes; and
f) repeating b), c), and d) after e) to
optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or
suggest these limitations for at least the same reasons
presented for Claim 1. Based at least on those reasons,
Applicants request reconsideration and withdrawal of the
rejection of Claim 3.

Claims 4-7 depends from Claim 3 and therefore are
patentable for at least the reasons presented for Claim 3.
Based on those reasons, Applicants also request reconsideration
and withdrawal of the rejection of Claims 4-7.


Claim 8, as amended, now recites:

a) placing cells of a circuit design by use
of non-direct timing driven processes;
b) routing wiring to connect said cells,
thereby generating a layout;
c) synthesizing said layout to optimize
timing;
d) performing an incremental placement of
said cells based on said synthesizing;
e) placing said cells by use of direct
timing driven placement processes; and
f) repeating b), c), and d) after e) to
optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or
suggest these limitations for at least the same reasons
presented for Claim 1. Based at least on those reasons,

Applicants request reconsideration and withdrawal of the rejection of Claim 8.

Claims 9-11 depends from Claim 8 and therefore are patentable for at least the reasons presented for Claim 8. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 9-11.

Claim 12, as amended, now recites:

a) synthesizing a high level description of a circuit to produce a circuit design;
b) placing cells of said circuit design by use of one of b1) non-direct timing driven processes and b2) direct timing driven processes;
c) routing wiring to connect said cells, thereby generating a layout;
d) modifying cell area allocations in said layout, if necessary to relieve congestion;
e) performing a post-layout synthesis optimization with said cells; and
f) providing an incremental placement of said cells,
wherein one of b1) and b2) is performed during a pass including c), d), e), and f),
wherein b1) is performed during a first pass, and wherein b2) is performed during any subsequent pass.

Applicant submits that Groenveld fails to disclose or suggest these limitations for at least the same reasons presented for Claim 1. Based at least on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 12.

Claims 13-18 depends from Claim 12 and therefore are patentable for at least the reasons presented for Claim 12. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claims 13-18.

Claim 19, as amended, now recites:

a processor coupled to a bus;

a memory coupled to said bus and wherein said memory contains instructions that when executed implement a method for placing circuit elements on an integrated circuit, said method comprising the steps of:

a) placing cells of a circuit design without regard to circuit timing;

b) providing routing information associated with said cells;

c) performing a detailed placement of said cells using said routing information;

d) placing said cells by use of direct timing driven placement processes; and

e) repeating b) and c) after d) to optimize placement of said cells.

Applicant submits that Groenveld fails to disclose or suggest these limitations for at least the same reasons presented for Claim 1. Based at least on those reasons, Applicants request reconsideration and withdrawal of the rejection of Claim 19.
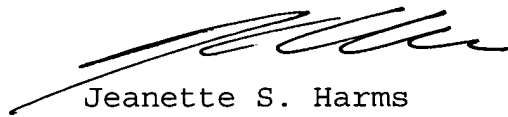
Claim 20 depends from Claim 19 and therefore is patentable for at least the reasons presented for Claim 19. Based on those reasons, Applicants also request reconsideration and withdrawal of the rejection of Claim 20.

## CONCLUSION

Claims 1-20 are pending in the present Application. Applicants respectfully request allowance of these claims.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 12, 2003.

8/12/03
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